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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,373	MURATA ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6,8,10-12,19,21,24-27,29,30,33 and 35-39* is/are rejected.

7)☒ Claim(s) *3,7,9,13-18,20,22,23,28,31,32 and 34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *26 August 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

2. Claims 13-23 are objected to because of the following informalities: the phrase "on one and same line" in claim 13 is grammatically incorrect. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 8, 19, 21, 33, and 39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. The term "almost equal" in claims 8, 19, 21, and 33 is a relative term which renders the claim indefinite. The term "almost equal" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

6. The examiner is unable to ascertain the exact tolerance with which "almost equal" is considered to be such by the specification and has therefore found the metes and bounds of these claims to be indefinite. Claims 8, 19, and 33 contain this phrase; claim 21 is dependent upon claim 19 and is therefore also found to be indefinite.

7. Claim 39 concludes with the phrase "the first connection being formed on the first wiring, and the second connection being formed on the first wiring and the projecting portion thereof." It is unclear to the examiner as to whether or not the applicant has intended to claim that the both the connections (the first and second) are formed on projecting portions of the first wiring. The examiner has interpreted the claim to mean that both the first and second connections are each formed on a projecting portion of the first wiring.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1, 2, 4-6, 8, 10-12, 24-27, 29, 30, 33, and 35-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Ema (USPN 5,014,104).

10. In reference to claim 1, Ema (USPN 5,014,104) discloses a similar method of fabrication. Figure 3(a) of Ema discloses a semiconductor device with a first wiring (G1 or G2) extending in a first direction and having at least one projecting portion. A second

wiring (N11 or N21) is connected to the first wiring (G1, G2 respectively) through a first connection and extends in a second direction orthogonal to the first direction. The second wiring (N11 or N21) has a surplus portion projecting from the connection in a direction opposite to the second direction. The first wiring (G1 or G2) and the second wiring (N11 or N21) are arranged such that the center of the connection is offset in the second direction from a center of the first wiring (G1 or G2) and a projecting portion of the first wiring (G1 or G2) is formed under the connection. The fabrication process for the device of figure 3(a) inherently meets the claimed method.

11. With regard to claim 2, Ema (USPN 5,014,104) discloses a similar method of fabrication. Figure 3(a) of Ema discloses a semiconductor device with a first wiring (G1) and a second wiring (G2) extending in a first direction which are adjacent to each other. A third wiring (N11) is connected to the first wiring (G1) through a first connection and extends in a second direction opposite to the second wiring (G2) and along a line orthogonal to the first direction. The third wiring (N11) has a first surplus projection projecting in the direction of the second wiring (G2) from the first connection. A fourth wiring (N21) is connected to the second wiring (G2) through a second connection and extends along the line in a direction opposite to the first wiring (G1). The fourth wiring (N21) has a second surplus projection projecting in the direction of the first wiring (G1) from the second connection. The first (G1), second (G2), third (N11), and fourth (N21) wirings are arranged such that the center of the second connection is offset in a direction opposite to the first wiring (G1) from a center of the second wiring (G2). The

second wiring (G2) has a projecting portion formed under the second connection. The fabrication process for the device of figure 3(a) inherently meets the claimed method.

12. In reference to claim 4, a fifth wiring (Vcc2 or Vss2) is formed in parallel with the third wiring (N11).

13. With regard to claim 5, the distance between the third wiring (N11) and the fifth wiring (Vcc2 or Vss2) is smaller than the distance between the first (G1) and second (G2) wirings.

14. In reference to claim 6, the distance between the first (G1) and the second (G2) wirings is larger than a minimum machining size.

15. So far as understood in claim 8, the width of each of the first (G1) and the second (G2) wirings and the width of each of the first and second connections are almost equal to each other.

16. With regard to claim 10, a MISFET underlies the first (G1) and second (G2) wirings. The second wiring (G2) is connected to a drain (Dp or Dn) of a MISFET.

17. With regard to claim 11, a center of the first connection is disposed on a center of the first wiring (G1).

18. In reference to claim 12, the first connection is formed so that a center is offset from a center of the first wiring (G1) in a direction opposite to the second wiring (G2). The first wiring (G1) has a projecting portion formed under the first connection.

19. In reference to claim 24, Ema (USPN 5,014,104) discloses a similar method of fabrication. Figure 3(a) of Ema discloses a semiconductor device with a first wiring (G1 or G2) extending in a first direction. There is a connection on the first wiring (G1 or G2).

A terminal (N11 or N21) on the connection extends in a second direction orthogonal to the first direction. The terminal (N11 or N21) has a surplus portion projecting from the connection in a direction opposite to the second direction. A second wiring (N11 or N21) extends in the second direction from the terminal (N11 or N21). The fabrication process for the device of figure 3(a) inherently meets the claimed method.

20. With regard to claim 25, Ema (USPN 5,014,104) discloses a similar method of fabrication. Figure 3(a) of Ema illustrates a plan view of a semiconductor device. There is a first wiring (G1 or G2) extending in a first direction. There is a second wiring (N11 or N21) extending in a second direction orthogonal to the first direction. The first wiring has (G1 or G2) has projecting portions respectively on both sides of an intersecting point of the first wiring (G1 or G2) and the second wiring (N11 or N21). Although not shown, it is understood that a first layout line of the first wiring layer (G1 or G2) and a second layout line of the second wiring layer (N11 or N21) are defined wherein the first wiring (G1 or G2) and the second wiring (N11 or N21) are disposed along there corresponding layout lines in order to arrive at the finished wiring structure shown in figure 3(a). A connection is disposed in an overlapped region of the first wiring (G1 or G2) and second wiring (N11 or N21) patterns. A pattern of the first wiring (G1 or G2) with the projecting portions is disposed only under the connection.

21. In reference to claim 26, Ema (USPN 5,014,104) discloses a similar device. Figure 3(a) of Ema discloses a semiconductor device with a first wiring (G1 or G2) extending in a first direction and having at least one projecting portion. A second wiring (N11 or N21) is connected to the first wiring (G1, G2 respectively) through a first

connection and extends in a second direction orthogonal to the first direction. The second wiring (N11 or N21) has a surplus portion projecting from the connection in a direction opposite to the second direction. The connection is formed so that a center is offset in the second direction from a center of the first wiring (G1 or G2). The first wiring (G1 or G2) has a projecting portion formed under the connection.

22. With regard to claim 27, Ema (USPN 5,014,104) discloses a similar device. Figure 3(a) of Ema discloses a semiconductor device with a first wiring (G1) and a second wiring (G2) extending in a first direction which are adjacent to each other. A third wiring (N11) is connected to the first wiring (G1) through a first connection and extends in a second direction orthogonal to the first direction and in opposition to the second wiring (G2). The third wiring (N11) has a first surplus projection projecting in the direction of the second wiring (G2) from the first connection. A fourth wiring (N21) is connected to the second wiring (G2) through a second connection and extends in a second direction orthogonal to the first direction and in opposition to the first wiring (G1). The fourth wiring (N21) has a second surplus projection projecting in the direction of the first wiring (G1) from the second connection. The second connection is formed so that a center is offset from a center of the second wiring (G2) in a direction opposite to the first wiring (G1). The second wiring (G2) has a projecting portion formed under the second connection.

23. In reference to claim 29, a fifth wiring (Vcc2 or Vss2) is formed in parallel with the third wiring (N11).

24. With regard to claim 30, the distance between the third wiring (N11) and the fifth wiring (Vcc2 or Vss2) is smaller than the distance between the first (G1) and second (G2) wirings.

25. So far as understood in claim 33, the width of each of the first (G1) and the second (G2) wirings and the width of each of the first and second connections are almost equal to each other.

26. With regard to claim 35, the second wiring (G2) is connected to a drain (Dp or Dn) of a MISFET.

27. With regard to claim 36, a center of the first connection is disposed on a center of the first wiring (G1).

28. In reference to claim 37, the first connection is formed so that a center is offset from a center of the first wiring (G1) in a direction opposite to the second wiring (G2). The first wiring (G1) has a projecting portion formed under the first connection.

29. In reference to claim 38, Ema (USPN 5,014,104) discloses a similar device. Figure 3(a) of Ema discloses a semiconductor device with a first wiring (G1 or G2) extending in a first direction and having at least one projecting portion. A second wiring (N11 or N21) is connected to the first wiring (G1, G2 respectively) through a first connection and extending from the first connection in a second direction orthogonal to the first direction. The second wiring has a first surplus portion projecting from the first connection in a direction opposite to the second direction. The first connection is formed on the first wiring (G1 or G2) and its projecting portion.

30. So far as understood in claim 39, Ema (USPN 5,014,104) discloses a similar device. Figure 3(a) of Ema discloses a semiconductor device with a first wiring (Vcc2 or Vss2) extending in a first direction and having at least one projecting portion. A second wiring (10 or 12 or 13) is connected to the first wiring (Vcc2 or Vss2) through a first connection and extends from the first connection in a second direction orthogonal to the first direction. The second wiring (10 or 12 or 13) has a first surplus portion projecting from the first connection in a direction opposite to the second direction. A third wiring (10 or 12 or 13) is connected to the first wiring (Vcc2 or Vss2) through a second connection and extends from the first connection in a second direction orthogonal to the first direction. The third wiring (10 or 12 or 13) has a second surplus portion projecting from the second connection in a direction opposite to the second direction. The first connection is formed on the first wiring (Vcc2 or Vss2) and its projecting portion while the second connection is formed on the first wiring (Vcc2 or Vss2) and its projecting portion.

Allowable Subject Matter

31. Claims 3, 7, 9, 28, 31, 32, and 34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

32. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests or renders obvious a semiconductor device having a two wiring layers extending in one direction and another

two wiring layers extending in a perpendicular direction relative to the first direction such that the first two wiring layers are connected to the second two wiring layers with the first two wiring layers having a slightly wider portion at an offset connection point and the second two wiring layers having an extra portion which extends past the offset connection point with the exact spacing and distance as specified by the applicant.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TC 2800

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